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Scotia Plaza, 40 King Street West, 40th Floor, Toronto, Ontario, Canada M5H 3Y2
Tel: 416.364.7311 Fax: 416.361.1398 www.bereskinparr.com

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FAX TRANSMITTAL

TO: Commissioner of Patents
FIRM: United States Patent and Trademark Office
FROM: Tony R. Orsi
FILE #: 11157-73
LAWYER #: 252

DATE: November 18, 2005 FAX #: 571-273-8300 PAGES: 5 (including cover sheet)

COMMENTS:

Please see attached Request for Correction of Filing Receipt

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November 18, 2005

Tony R. Orsi
B.A.Sc., M.A.Sc. (Elec. Eng.)
416 957 1603 torsi@bereskinparr.com

Your Reference: 10/788,491
Our Reference: 11157-73

By Fax 1-571-273-8300

REQUEST FOR CORRECTION OF FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia
22313-1450

Dear Sir:

Re: United States Patent Application No. 10/788,491
For: WIRELESS RADIO FREQUENCY TECHNIQUE DESIGN AND METHOD FOR TESTING OF INTEGRATED CIRCUITS AND WAFERS
Filing Date: March 1, 2004
Applicant: MOORE, Brian

This is further to the Filing Receipt dated May 19, 2004 for the above-noted patent application. Applicant notes an error on the filing receipt under the heading "title". The title should be "Wireless Radio Frequency Technique Design and Method For Testing of Integrated Circuits and Wafers".

A copy of the filing receipt with the correction in the title is attached.

A copy of the first page of the application, as filed, is also attached for your reference.

We look forward to receiving a corrected filing receipt incorporating the change.

Respectfully submitted,

Tony R. Orsi
Registration No. 55,831
/cem
Encl.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/788,491	03/01/2004	2858	853	11157-073	22	72	3

CONFIRMATION NO. 7561

001059
BERESKIN AND PARR
SCOTIA PLAZA
40 KING STREET WEST-SUITE 4000 BOX 401
TORONTO, ON M5H 3Y2
CANADA

FILING RECEIPT

OC000000012712706

Date Mailed: 05/19/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Brian Moore, Edmonton, CANADA;

Assignment For Published Patent Application

The Governors of The University of Alberta, Edmonton, CANADA;

Domestic Priority data as claimed by applicant

This application is a CON of 09/854,905 05/15/2001

Foreign Applications

CANADA 2,308,820 05/15/2000

If Required, Foreign Filing License Granted: 05/19/2004

Projected Publication Date: 08/26/2004

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Wireless radio frequency technique design and method for testing of integrated circuits and wafers

Preliminary Class
324

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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Title: Wireless Radio Frequency Technique Design And Method For Testing Of Integrated Circuits And Wafers

This application is a continuation of prior Application No. 09/854,905, filed May 15, 2001, the entirety of which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for the testing of wafers during the IC fabrication process and more particularly to a method and apparatus for the wireless testing of ICs on wafers.

BACKGROUND OF THE INVENTION

In the Integrated Circuit (IC) manufacturing process, a plurality of ICs are formed upon the surface of a circular wafer by the successive deposition of various materials such as metal and oxide layers according to a design layout. After all of the layers have been deposited, the wafer is diced into separate ICs that are then packaged for sale. For quality assurance purposes and for evaluating the manufacturing process, the ICs are tested for proper operation before they are packaged for sale. However, if it could be determined before dicing and packaging that a defect had occurred in a particular IC, or in the manufacturing process, then substantial cost savings could be achieved by discarding the damaged IC before it is packaged or by discarding the entire wafer before it is diced and making corrections to the manufacturing process.

Conventional IC testing is done after all of the layers have been deposited on the wafer. Due to imperfections in the manufacturing process, a certain amount of the ICs will be defective. For instance if the probability of a defect occurring during the deposition of a metallization layer is 1% then the probability of having defective ICs after 7 metallization layers have been deposited is 6.8% which is not insignificant since ICs are mass produced in large quantities. This is an investment on the part of the manufactures that could be mitigated by knowing errors in the manufacturing process before other manufacturing steps are done. Furthermore, because subsequent metallization layers affect the operation of previous metallization layers, it is